What is claimed is:

- 1 1. A simultaneous bidirectional port circuit comprising:
- a sampling circuit configured to sample an incoming waveform;
- a receiver coupled to the sampling circuit configured to measure an
- 4 amplitude of the incoming waveform;
- a storage mechanism to store information from the receiver; and
- a control mechanism configured to control the receiver and the sampling
- 7 circuit to measure the amplitude of a repetitive incoming waveform at a plurality of
- 8 time points.
- 1 2. The simultaneous bidirectional port circuit of claim 1 wherein the receiver
- 2 comprises a variable offset comparator.
- 1 3. The simultaneous bidirectional port circuit of claim 1 wherein the storage
- 2 mechanism comprises a counter.
- 1 4. The simultaneous bidirectional port circuit of claim 1 wherein the storage
- 2 mechanism comprises a shift register.
- 1 5. The simultaneous bidirectional port circuit of claim 1 further comprising an
- 2 output driver having an output node coupled to an input node of the sampling
- 3 circuit.
- 1 6. The simultaneous bidirectional port circuit of claim 1 wherein:
- the receiver comprises a comparator; and
- the simultaneous bidirectional port circuit further comprises a variable
- 4 reference coupled to the comparator.

- The simultaneous bidirectional port circuit of claim 1 wherein the control
- 2 mechanism is configured to calculate a distribution for each of the plurality of time
- 3 points.
- 1 8. An integrated circuit comprising:
- a signal node to receive a data signal; and
- a port circuit coupled to the signal node, the port circuit configured to
- 4 receive digital data from the signal node during a first mode of operation, and
- 5 configured to capture a waveform of a signal on the signal node during a second
- 6 mode of operation.
- 1 9. The integrated circuit of claim 8 wherein the port circuit comprises a
- 2 variable offset comparator having an input node coupled to the signal node.
- 1 10. The integrated circuit of claim 8 wherein the port circuit comprises an output
- 2 driver having an output coupled to the signal node.
- 1 11. The integrated circuit of claim 10 wherein the port circuit is configured as a
- 2 simultaneous bidirectional port circuit.
- 1 12. The integrated circuit of claim 8 further comprising a clock input node to
- 2 receive a clock signal.
- 1 13. The integrated circuit of claim 12 wherein the port circuit further comprises
- a sampling circuit coupled to the clock input node to sample the signal on the signal
- 3 node at various time points.
- 1 14. The integrated circuit of claim 13 further comprising a storage mechanism to
- 2 store information describing the waveform of the signal.

- 1 15. The integrated circuit of claim 14 wherein the storage mechanism comprises
- 2 a counter.
- 1 16. The integrated circuit of claim 14 wherein the storage mechanism comprises
- 2 a shift register.
- 1 17. An electronic system comprising:
- an integrated circuit including a signal node to receive a signal, and a port
- 3 circuit coupled to the signal node, the port circuit configured to receive digital data
- 4 from the signal node during a first mode of operation, and configured to capture a
- 5 waveform of the signal on the signal node during a second mode of operation; and
- a network interface capable of coupling the integrated circuit to a network.
- 1 18. The electronic system of claim 17 wherein the port circuit comprises a
- 2 variable offset comparator having an input node coupled to the signal node.
- 1 19. The electronic system of claim 17 wherein the port circuit comprises an
- 2 output driver having an output coupled to the signal node.
- 1 20. The electronic system of claim 17 wherein the port circuit comprises a
- 2 sampling circuit to sample the signal on the signal node at various time points.
- 1 21. A method of capturing a waveform on an integrated circuit die comprising:
- 2 sampling a simultaneous bidirectional data signal at a first time point;
- receiving the simultaneous bidirectional data signal at a receiver; and
- 4 varying a threshold of the receiver.
- 1 22. The method of claim 21 wherein sampling comprises subtracting an
- 2 outgoing signal from an incoming signal.

- 1 23. The method of claim 21 wherein receiving comprises receiving the
- 2 simultaneous bidirectional data signal at a variable offset comparator.
- 1 24. The method of claim 23 wherein varying a threshold comprises varying an
- 2 offset of the variable offset comparator.
- 1 25. The method of claim 24 further comprising:
- 2 sampling the simultaneous bidirectional data signal at a plurality of time
- 3 points; and
- 4 varying the offset of the variable offset comparator at each of the plurality of
- 5 time points.
- 1 26. The method of claim 21 wherein the simultaneous bidirectional data signal is
- 2 repetitive, and sampling at a first time point comprises taking a plurality of samples
- at substantially the same time with respect to the repetitive signal.
- 1 27. The method of claim 26 further comprising varying the threshold during the
- 2 plurality of samples.
- 1 28. A method comprising:
- 2 receiving a signal at a receiver configured to receive digital data and
- 3 configured to capture a waveform of the signal;
- 4 sampling the signal at a plurality of time points; and
- 5 varying a threshold of the receiver at each of the plurality of time points.
- 1 29. The method of claim 28 wherein the signal is repetitive, and wherein
- 2 sampling comprises sampling the repetitive signal more than once at each of the
- 3 plurality of time points.
- 1 30. The method of claim 29 wherein:

- 2 receiving comprises receiving the signal at a variable offset comparator; and
- varying a threshold of the receiver comprises varying an offset of the
- 4 variable offset comparator.